REMARKS

Claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58 and 80-85 are pending in this application. Claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58 and 80-85 have been rejected. By this paper, the Applicant amends claims 1, 4, 6, 8-11, 13, 14, 20, 23, 25, 27-30, 32, 33, 38, 41, 43, 45-48, 50 and 51 for clarification. No new matter has been added.

At ¶2 of the Office Action, the Examiner objects to the disclosure because of informalities in paragraphs [003] and [004]. Accordingly, the applicant has amended those paragraphs, so those objections should be withdrawn.

At ¶5 of the Office Action, the Examiner rejects claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58 and 80-85 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1, 20 and 38, the Applicant amends those claims to recite, "nodes" rather than "IR nodes." Claims 9, 14, 28, 33, 46 and 51 have been amended to correspond to the amendments of claims 1, 20 and 38.

Regarding claims 4, 23 and 41, the Applicant amends those claims to recite, "the base nodes" rather than "base nodes." Regarding claims 6, 8, 25, 27, 43 and 45, the Applicant amends those claims to recite, "the complex nodes" rather than "complex nodes."

Regarding claims 10, 11, 13, 29, 30, 32, 47, 48 and 50, the Applicant amends those claims to recite, "the polymorphic nodes" rather than "polymorphic nodes."

Accordingly, the rejections of claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58 and 80-85 under 35 U.S.C. 112, second paragraph should be withdrawn.

At ¶7 of the Office Action, the Examiner rejects claims 1, 4, 7, 8, 14-18, 20, 23, 26, 27, 33-38, 41, 44, 45, 51-55 and 83 under 35 U.S.C. 102(b) as being anticipated by WO 00/22521

(Souloglou). The Applicant traverses these rejections, and submits that independent claims 1, 20 & 38 are not anticipated by Souloglou.

The Souloglou Reference

Pages 1 and 2 of Souloglou discuss basic concepts in the field of program code conversion such as dividing a subject program into "Basic Blocks", where each of these basic blocks is a sequence of instructions that has only one entry point at a first instruction of the block and only one exit point at a last instruction of the block.

As noted on page 4 of the Office Action, Souloglou further discloses that program code written for a particular type of subject processor is translated block by block into program code for a target processor via an intermediate representation. See page 2, second full paragraph:

> In an alternative form of emulation, a program in code of a subject processor (i.e., a first type of processor for which the code is written and which is to be emulated) is translated in Basic Blocks, via an intermediate representation, into code of a target processor (i.,e., a second type of processor on which the emulation is performed).

The intermediate representation of Souloglou is discussed in detail on pages 17-21 with reference to Figures 1-5. That is, each basic block of instructions is broken down to produce "register objects" and "expression objects" arranged in a directed acyclic graph (DAG or "tree") as an intermediate representation of the basic block of program code instructions.

The Examiner refers particularly to page 11, lines 21-26, page 13, first paragraph and page 5, last 4-5 lines of Souloglou. These selected portions of Souloglou are each concerned with a further optimization of the intermediate representation where the subject code is written for a special type of processor that has "variable-sized registers." Here, it is important to appreciate that the "variable sized register" mentioned in Souloglou means a register which is addressable by the subject code in a plurality of different widths, as shown particularly in Souloglou at page 7, third paragraph:

> An example of an instruction-set which uses a variable-sized register is the Motorola 68000 architecture. In the 68000 architecture, instructions that are specified as'long' (. 1). operate on all 32 bits of a register or memory location. Instructions that are specified as'word' (. w). or'byte' (. b). operate on only the bottom 16 and bottom 8 bits respectively, of a register or memory location. Even if a byte addition, for example, generates a carry, that carry is not propagated into the 9th bit of the register.

The referenced portions of Souloglou on pages 5, 11 and 13 discuss the building of intermediate representation by referring to an "associated set of register objects" each of which represents a different width of the variable-sized register. This leads to the elimination of redundancies in the intermediate representation and allows target code to be produced from the intermediate representation which functions more efficiently on a target (host) processor, especially when that target processor does not itself provide such variable-sized registers.

It is clear that Souloglou does not disclose generating intermediate representation having both "base nodes" and "complex nodes" as in the claimed invention. In particular, Souloglou does not disclose at least the following features from independent claims 1, 20 & 38:

> "providing a plurality of nodes in the intermediate representation as abstract representations of the expressions, calculations, and operations performed by the instructions of the subject code
>
> [wherein the nodes are] selected from a plurality of possible types of nodes including at least base nodes and complex nodes,
>
> wherein the base nodes represent the most basic semantics of the subject code such that the semantics of base nodes cannot be decomposed into other nodes representing more simple semantics, and
>
> wherein the complex nodes provide a more compact representation of the semantics of complex instructions in the program code than that of base node representations"

On the contrary, Souloglou only discloses the equivalent of "base nodes" in the claimed invention. There is no disclosure in Souloglou of anything equivalent to the "complex nodes" the applicant discloses and claims. Souloglou only discloses breaking down a complex instruction (e.g., a CISC instruction) into a plurality of base nodes. By contrast, the claimed invention recites that this one complex instruction is instead represented by one "complex node" in the intermediate representation and is not decomposed into a plurality of base nodes.

The claimed invention is a significant improvement over the prior art of Souloglou, because the claimed invention provides not only "base nodes" like Souloglou but also provides the "complex nodes" which provide a more compact representation of the semantics of complex instructions in the subject program code than the representation provided just by the base nodes alone.

Paragraph [004] of the present application (paragraph [0006] of the corresponding publication US 2004/02212277 A1) specifically acknowledges the published prior art of US 09/827,971 which is directly derived from the cited Souloglou WO reference. Figures 1-5 of the present application are the same as the Souloglou reference, because this helps the person of ordinary skill in the art to understand that Souloglou discloses the equivalent of "base nodes" in the present invention. However, it is also readily understood that Souloglou does not disclose anything equivalent to "complex nodes" of the claimed invention.

The Applicant also respectfully disagrees with the rejections of the dependent claims, which recite further novel and non-obvious features of the invention. The comments in the Office Action concerning the dependent claims are incorrect, not least because the Office Action has incorrectly interpreted the disclose of Souloglou with reference to the independent claims 1, 20 & 38.

For at least the reasons set forth above, Souloglou does not teach or suggest all of the elements of independent claims 1, 20 and 38, so those rejections are improper and should be withdrawn. Claims 4, 7, 8, 14-18, 23, 26, 27, 33-37, 41, 44, 45, 51-55 and 83 each depends from an allowable base claim 1, 20 or 38, so those claims should also be allowable.

At ¶9 of the Office Action, the Examiner rejects claims 6, 25 and 43 under 35 U.S.C. 103(a) as being unpatentable over Souloglou in view of U.S. Patent No. 6,292,935 (Lueh). The Applicant traverses this rejection.

Lueh does not disclose generating the intermediate representation to further include "polymorphic nodes," as recited in the dependent claims 9, 28 and 43. Lueh at column 5, lines 7-31 cited in the Office Action discusses pushing operands onto a "mimic stack" including register

operands, intermediate operands, memory operands and floating point operands obtained from operand stack based source code. The "mimic stack" is a stack that the compiler of Lueh uses to keep track of operands that have been pushed onto the operand stack by the operand stack based source code. There is no "intermediate representation" in Lueh. Thus, it is improper to combine the mimic stack of Lueh with intermediate representation as in Souloglou. Further, such a combination still does not arrive at "polymorphic nodes" as in the dependent claims 9, 28 and 43.

Since Souloglou and Lueh do not teach or suggest all of the limitations of claims 9, 28 and 43, alone or in combination, these rejections are improper and should be withdrawn.

At ¶10 of the Office Action, the Examiner rejects claims 9-13, 28-32, 46-50, 56-58, 80-82 and 84-85 under 35 U.S.C. 103(a) as being unpatentable over Souloglou in view of "The LLVM Instruction Set and Compilation Strategy" (Lattner). The Applicant traverses this rejection. Combining Souloglou with Lattner does not teach or suggest the specific features of the "polymorphic nodes" recited in any of the dependent claims 9-13, 28-32, 46-50, 56-58, 80-82 and 84-85.

As noted at page 10 of the Office Action, Lattner uses the word "polymorphic" for example at page 4, section 3.2. Lattner discloses a compiler using a low level virtual machine (LLVM) having a low-level virtual machine instruction set. As noted at Section 3.2, the LLVM instructions are polymorphic in that a single instruction like "add" can operate on several different types of operands. However, the polymorphic LLVM instructions of Lattner are clearly totally unrelated to the "polymorphic nodes" within the intermediate representation recited by the claimed invention. For example, the Applicant draws attention specifically to dependent claims 10, 29 and 47 each of which recite that:

> ". . . the polymorphic nodes each contain a function pointer to a function of the target architecture specific to a particular instruction in the subject code."

Thus, claims 9-13, 28-32, 46-50, 56-58, 80-82 and 84-85 are not obvious in view of the combination of Souloglou and Leuh, or Souloglou and Lattner, since none of these combinations

teaches or suggests all of the limitations of the claims. Accordingly, those rejections are improper and should be withdrawn.

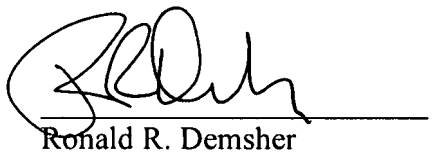
In summary, the specification and the claims have been amended for clarity in response to the comments in the Office Action. Concerning the rejections related to novelty and obviousness, the Applicant respectfully submits that there are clear differences between the "base nodes" of Souloglou, the "mimic stack" of Lueh and the "polymorphic LLVM instructions" in the compiler of Lattner, and it is impossible to derive all of the recited features of the claimed invention from any combination of the cited documents.

Filed herewith is a Request for a One-Month Extension of Time, which extends the statutory period for response to expire on August 12, 2007. Accordingly, Applicant respectfully submits that this response is being timely filed.

In view of the above amendment, applicant believes the pending application is in condition for allowance. No other fees are believed to be due in connection with the filing of this response, however the Commissioner is authorized to debit Deposit Account No. 08-0219 for any required fee necessary to maintain the pendency of this application.

Respectfully submitted,

Dated: August 13, 2007



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